REMARKS

I. Introduction

In response to the Office Action dated November 29, 2006, Applicants have amended claims 1 and 4 – 8 to more particularly point out and distinctly claim the subject matter of the invention. Care has been taken to avoid the introduction of new matter. In view of the foregoing amendments and the following remarks, Applicants respectfully submit that all pending claims are in condition for allowance.

II. Objections to the Specification

The Examiner asserts that the sentence structure of the recitation on page 1, lines 6 – 8 of the specification is "grammatically incomprehensible." Applicants have amended this portion of the specification to more clearly recite the relationship between a device associated with a program owner and a device associated with a program user. Withdrawal of this objection is respectfully solicited.

III. Claim Rejections Under 35 U.S.C. § 112

Claims 1 – 8 stand rejected under 35 U.S.C. § 112, second paragraph, as allegedly being "generally narrative and indefinite." The Examiner points specifically to the recitation of a controller in claim 1. Applicants have amended claims 1 and 6 to more clearly define the controller. If the Examiner still considers other claim recitations to be indefinite, Applicants request that the Examiner identify those recitations so that Applicants can appropriately address them. Withdrawal of this rejection is respectfully solicited.

IV. Claim Rejections Under 35 U.S.C. § 103

Claims 1, 2, 4, and 5 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Saito (U.S. Patent No. 8,438,694) in view of Nara (U.S. Patent No. 5,168,151). Claims 3, 6, and 8 stand rejected under § 103 as being unpatentable over Saito, Nara, and the allegedly Admitted Prior Art. Claim 7 stands rejected under § 103(a) as being unpatentable over Saito in view of the allegedly Admitted Prior Art. Applicants traverse these rejections for at least the following reasons.

Claim 1 recites, among other things, a semiconductor integrated circuit device comprising a first RAM for inputting and outputting data between a bus and itself, a second RAM for inputting and outputting data between a bus and itself, and a controller for causing a bus port to disable access from the outside when an encrypted program and the decryption program are stored in the first RAM. At least these features are not disclosed or suggested by any of the cited references, taken alone or in combination with each other.

Saito fails to disclose a first and second RAM. While the semiconductor device of Saito does include one RAM (RAM 19, depicted in Figure 3), it does not include a second RAM. Rather, Saito disclose using a ROM (ROM 18, depicted in Figure 3) as a memory element. However, the ROM stores read-only data, which cannot be overwritten like the RAM recited in claim 1. Thus, Saito fails to disclose this element of the pending claims. Nara is not relied upon as curing this deficiency.

The Examiner correctly acknowledges that Saito does not disclose a controller for causing the bus port to disable access from the outside when an encrypted program and the decryption program are stored in the first RAM, and relies on Nara to overcome this rejection. The controller recited in claim 1 is configured to control reading and writing to both the first and second RAMs. The memory controller 40 disclosed by Nara appears to control the retrieval of

data from an IC card to the outside, but does not disclose or even suggest controlling the reading and writing of data between two RAMs in the IC card.

Accordingly, as each and every limitation must be disclosed or suggested by the prior art references in order to establish a *prima facie* case of obviousness (MPEP § 2143.03), and Saito and Nara, alone or in combination with each other, do not disclose or even suggest at least the features recited above, it is respectfully submitted that independent claims 1 is patentable over the cited references.

Independent claims 6 – 8 each include features similar to those described above in relation to claim 1. Accordingly, these claims are patentable over the cited references for at least the reasons provided above in reference to claim 1. Claims 2 – 5 depend from independent claim 1. Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Harness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claim 1 is patentable for at least the reasons set forth above, it is respectfully submitted that all dependent claims are also in condition for allowance. In addition, it is respectfully submitted that the dependent claims are patentable based on their own merits by adding novel and non-obvious features to the combination

V. Conclusion

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Michael E. Fogarty
Registration No. 36,139

Please recognize our Customer No. 53080 as our correspondence address.

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF:DAB
Facsimile: 202.756.8087
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